Amendments to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the above-identified application.

Listing of Claims:

1-17. (Cancelled)

18. (Currently amended) A microinstruction sequencer, comprising:

a microinstruction sequencer stack comprising an array of memory cells; and

microinstruction sequencing logic associated with the microinstruction sequencer stack, wherein the microinstruction sequencing logic is responsive to an operation code that includes ~~determines if a microinstruction affects the microinstruction sequencer stack by determining if operation code is present in a~~ first field for non-microinstruction sequencer stack operations ~~in the microinstruction~~ and a second field ~~reserved~~ for microinstruction sequencer stack operations.

19. (Currently amended) A microprocessor including a microinstruction sequencer, comprising:

an array of memory cells dedicated to a microinstruction sequencer stack;

an address multiplexer coupled to said array of memory cells;

sequencing logic coupled to the address multiplexer and to the array of memory cells, wherein the sequencing logic is responsive to an operation code that includes ~~determines if a microinstruction affects the microinstruction sequencer stack by determining if operation code is present in a~~ first field for non-microinstruction sequencer stack operations ~~in the microinstruction~~ and a second field~~reserved~~ for microinstruction sequencer stack operations; and

a microprocessor core unit coupled to the array of memory cells.

20. (Previously Presented) The microinstruction sequencer of claim 18, wherein the microinstruction includes instructions to:

generate a value of a microinstruction address;

add an intermediary value to the value of the microinstruction address to yield an

incremented value;

send a control value to the microinstruction sequencer stack, said control value to cause the incremented value to be pushed onto the microinstruction sequencer stack; and

push the incremented value onto the microinstruction sequencer stack.

21. (Currently amended) The microinstruction sequencer of claim 18, wherein the microinstruction ~~sequencing logic~~ includes ~~logic~~ instructions to:

send a control value to the microinstruction sequencer stack, said control value to:

cause the microinstruction sequencer stack to pop a value; and

send the popped value to a microinstruction address multiplexer.

22. (Currently amended) The microinstruction sequencer of claim 18, wherein the microinstruction ~~sequencing logic~~ includes ~~logic~~ instructions to:

send a control value to the microinstruction sequencer stack, said control value to:

cause the microinstruction sequencer stack to pop a value; and

send the popped value to an immediate logic, said immediate logic to pass the value to a microprocessor core unit.

23. (Currently amended) The microinstruction sequencer of claim 18, wherein the microinstruction ~~sequencing logic~~ includes ~~logic~~ instructions to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to push a value in an immediate field of a microinstruction onto the microinstruction sequencer stack.

24. (Currently amended) The microinstruction sequencer of claim 18, wherein the microinstruction ~~sequencing logic~~ includes instructions ~~logic~~ to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to return to a reset state.

25. (Currently amended) The microinstruction sequencer of claim 18, wherein the microinstruction ~~sequencing logic~~ includes ~~logic~~ instructions to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer

stack to pop a value and send the popped value to an immediate logic.

26. (Currently amended) The microinstruction sequencer of claim 18, wherein the microinstruction ~~sequencing logic~~ includes ~~logic~~ instructions to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to send a value at the top of the microinstruction sequencer stack to an immediate logic.

27. (Previously presented) The microinstruction sequencer of claim 19, wherein the microprocessor core unit is an execution unit.

28. (Previously presented) The microinstruction sequencer of claim 19, wherein the microprocessor core unit is a retire unit.